What is claimed is:

1. A buffer layer, suitable for a substrate of a thin film transistor (TFT), comprising:

an amorphous layer, deposited on the substrate; and

an oxide-containing layer, deposited on the amorphous silicon layer.

2. The buffer layer as claimed in claim 1, wherein the oxide-containing layer comprises silicon oxide (SiO_x).

3. The buffer layer as claimed in claim 1, wherein the oxide-containing layer is a crystallized layer.

4. The buffer layer as claimed in claim 1, wherein the thickness of the oxide-containing layer is about 1000~2000Å.

5. The buffer layer as claimed in claim 1, wherein the oxide-containing layer is formed by plasma enhanced chemical vapor deposition (PECVD).

6. The buffer layer as claimed in claim 1, wherein the density of the oxide-containing layer is about 2.0~2.2 g/cm^3.

7. The buffer layer as claimed in claim 1, wherein the amorphous layer comprises amorphous silicon.

8. The buffer layer as claimed in claim 1, wherein the thickness of the amorphous layer is about 250~1000Å.

9. The buffer layer as claimed in claim 1, wherein the density of the amorphous layer is about 2.0~2.3 g/cm^3.

10. The buffer layer as claimed in claim 1, wherein the hydrogen content of the amorphous layer is about 5~10%.

11. The buffer layer as claimed in claim 1, wherein the amorphous layer is formed by plasma enhanced chemical vapor deposition (PECVD).

12. The buffer layer as claimed in claim 1, wherein the buffer layer further comprises a nitride layer deposited between the substrate and the amorphous layer.

13. The buffer layer as claimed in claim 12, wherein the nitride layer comprises silicon nitride.

14. The buffer layer as claimed in claim 1, wherein the hydrogen content of the amorphous layer is less than 10%.

15. A thin film transistor having a buffer layer for promoting electron mobility, comprising:

a substrate;

a buffer layer, comprising:

an amorphous layer, deposited on the substrate; and

a crystallized layer, deposited on the amorphous layer;

an active layer, deposited on the crystallized layer;

an insulating layer, covered conformally on the active layer, the amorphous layer, crystallized layer and the side walls of the active layer;

a conductive layer, deposited on the insulating layer above parts of the active layer; and

a dielectric layer, completely covering the crystallized layer and the conductive layer.

16. The buffer layer as claimed in claim 15, wherein the crystallized layer comprises oxide.

17. The buffer layer as claimed in claim 15, wherein the thickness of the crystallized layer is about 1000~2000Å.

18. The buffer layer as claimed in claim 15, wherein the amorphous layer comprises amorphous silicon.

19. The buffer layer as claimed in claim 15, wherein the thickness of the amorphous layer is about 1000~2000Å.

20. The buffer layer as claimed in claim 15, wherein the hydrogen content of the amorphous layer is less than 10%.

21. The buffer layer as claimed in claim 15, wherein the buffer layer further comprises silicon nitride deposited between the substrate and the amorphous layer.